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1 Atomic layer deposition of high-/spl kappa/ dielectric for germanium MOS applications - substrate
Chi On Chui; Kim, H.; McIntyre, P.C.; Saraswat, K.C.;

Electron Device Letters, IEEE , Volume: 25 , Issue: 5 , May 2004

Pages:274 - 276

[\[Abstract\]](#) [\[PDF Full-Text \(168 KB\)\]](#) **IEEE JNL**
2 Charge trapping in ultrathin hafnium oxide
Zhu, W.J.; Ma, T.P.; Zafar, S.; Tamagawa, T.;

Electron Device Letters, IEEE , Volume: 23 , Issue: 10 , Oct. 2002

Pages:597 - 599

[\[Abstract\]](#) [\[PDF Full-Text \(201 KB\)\]](#) **IEEE JNL**
3 Atomic layer deposition of high-k thin films for gate and capacitor dielectrics
Senzaki, Y.; Chatham, H.; Park, S.; Bartholomew, L.; Lo, T.; Okuyama, Y.; Ba C.; Tousseau, C.; Fleming, T.; Ford, B.;

Integrated Circuit Design and Technology, 2004. ICICDT '04. International Conference on , 2004

Pages:269 - 274

[\[Abstract\]](#) [\[PDF Full-Text \(582 KB\)\]](#) **IEEE CNF**
4 Influence of metal gate materials and processing on planar CMOS device characteristics with high-k gate dielectrics
Majhi, P.; Young, C.; Bersuker, G.; Wen, H.C.; Brown, G.A.; Foran, B.; Choi, I. Zeitsoff, P.M.; Huff, H.R.;

Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of